BIDIRECTIONAL SHIFT REGISTER

Bidirectional shift registers: Bidirectional shift registers are the registers which are capable of shifting the data either right or left depending on the mode selected. If the mode selected is 1 (high), the data will be shifted towards the right direction and if the mode selected is 0 (low), the data will be shifted towards the left direction.

If the data is shifted towards right by one position, then it is equivalent to ~~dividing~~ dividing original number by 2. and conversely if the binary no. is shifted left by one bit position then, it is equivalent to multiplying the original number by 2.

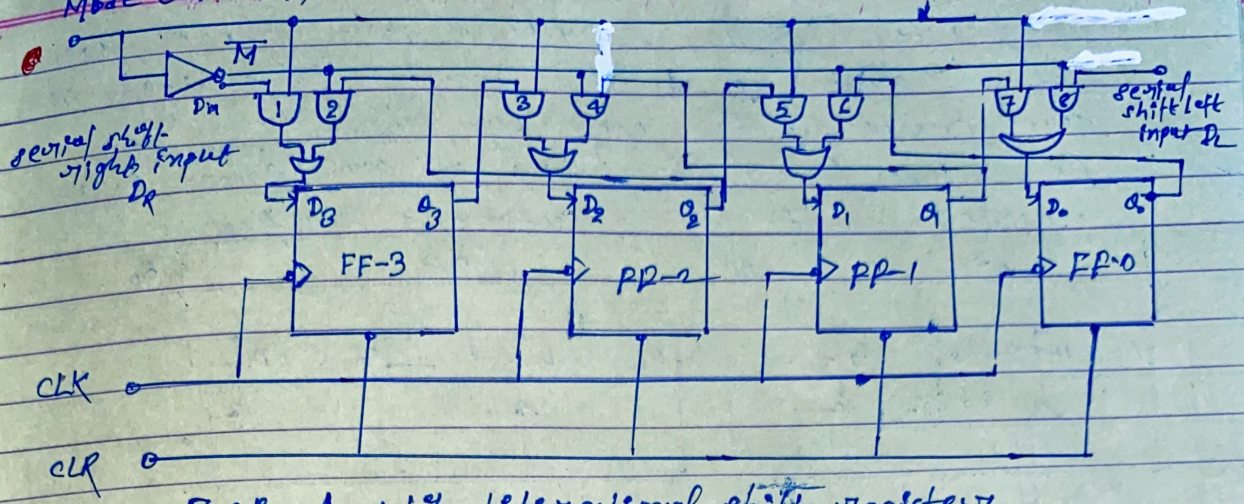


Fig: A-4 bit bidirectional shift register.

Here, there are two inputs i) serial right shift data input D_R and serial left shift data input D_L along with a Mode select input (M).

Working operation:

I) with M=1: shift right operation:

If M=1, then AND gates 1, 2, 5 and 7 are enabled whereas the remaining AND gate 3, 4, 6 and 8 will be disabled. Hence the data at D_R is shifted to right bit-by-bit from FF-3 to FF-0 upon the application of clock pulse. Thus we get serial shift right operation.

II) with M=0: shift left operation: when the mode control M is connected to 0 then AND gates 3, 4, 6 and 8 are enabled while 1, 2, 5, 7 are disabled. Hence the data at D_L will shift the data bit by bit from FF-0 to FF-3 on the application of clock pulse.

BUFFER REGISTERS

Buffer registers: Buffer registers are type of registers used to store a binary word. These registers are constructed by using flip-flops.
The below figured shows a 4-bit synchronous buffer register formed by cascading 4 flip flops.

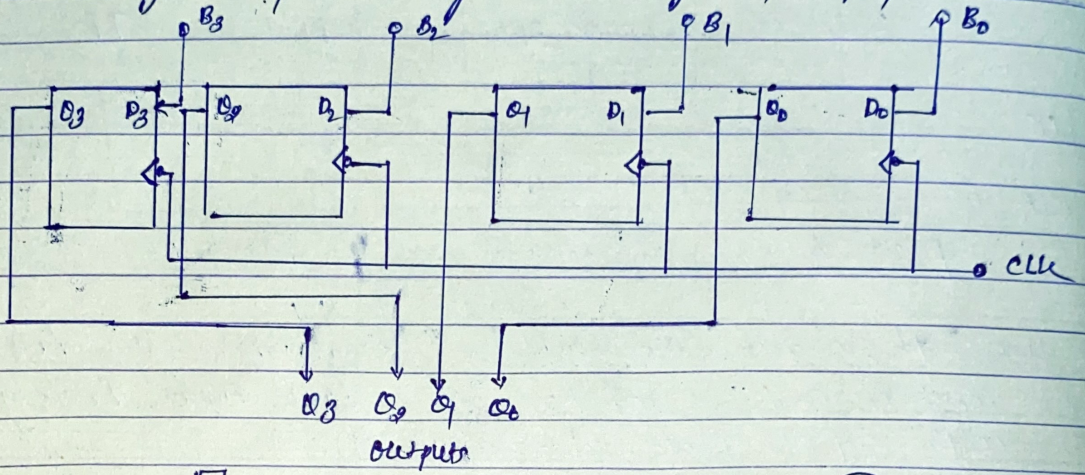


Fig - 4-bit Buffer register using D-flip flops

working

Let $B_3B_2B_1B_0$ = 1010 is to be stored. These bits are connected to the D inputs of four D flip flops. Now when we apply clock pulse then, with the 1st raising edge of clock signal (pulse), The outputs are $Q_3Q_2Q_1Q_0$ = 1010.

Conclusion:

i) To store n-bit we require n flip-flops.
ii) As the data bits are loaded simultaneously and output is taken simultaneously, it is also called PIPO and operation is called parallel shifting.

Application:

i) For temporary data storage
ii) For multiplication and division
iii) As a delay line.
iv) As serial to parallel converter.

V) As parallel to serial converter.
VI) As ring counter.
VII) As twisted ring counter or Johnson counter

RING COUNTER

Ring counter :- Ring counter is a typical application of shift register. Ring counter is almost same as the shift counter.
A ring counter is a type of counter composed of flip-flops connected into a shift register, with the output of the last flip-flop fed to the input of the first, making a "circular" or ring structure.

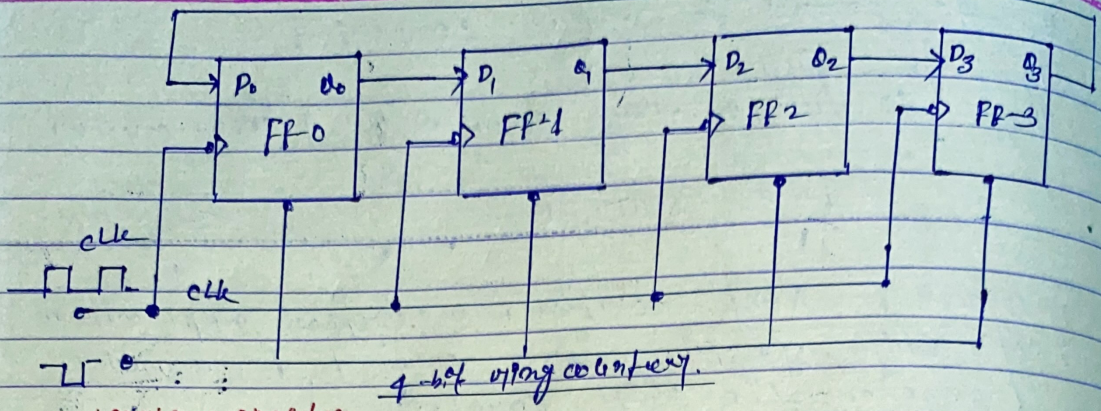
Type of ring counter:

There are two types of ring counter:

I) A straight ring counter: It is also known as one-hot counter, connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring.

II) A twisted ring counter: A twisted ring counter, also called switch-tail ring, ring counter, walking ring counter, Johnson counter or Mobius counter, connects the complement of the output of the last shift register to the input of first register and circulates a stream of ones followed by zeros around the ring.

1) Ring counter (A straight ring counter) :- The figure shown on the overleaf page is the correct diagram of ring counter.



4-bit ring counter.

Working operation:

Initially a low clear (CLR) pulse is applied to all the flip-flops. this clears all outputs to 0

i.e $Q_0 Q_1 Q_2 Q_3 = 0000$

Now, Apply 1 to D_0 then,

1) On the first -ve edge clk edge.

As soon as the first falling edge of the clock hits, the FF-0 only get set and remaining FF states are 0.

i.e $Q_0 Q_1 Q_2 Q_3 = 1000$

2) On the second falling edge of clock.

with the second falling edge of clock signal FF-1 goes to set and remaining are of reset

i.e $Q_0 Q_1 Q_2 Q_3 = 0100$

Similarly on third falling edge,

$Q_0 Q_1 Q_2 Q_3 = 0010$

- On fourth falling edge,

$Q_0 Q_1 Q_2 Q_3 = 0001$

on fifth falling edge, $Q_0 Q_1 Q_2 Q_3 = 1000$

So. The number of output states for a ring counter will always be equal to the number of flip-flops.

Truth Table:

CLR	clk	Q_0	Q_1	Q_2	Q_3
↓	X	0	0	0	0
↑	↓	1	0	0	0
↑	↓	0	1	0	0
↑	↓	0	0	1	0
↑	↓	0	0	0	1
⋮	⋮				

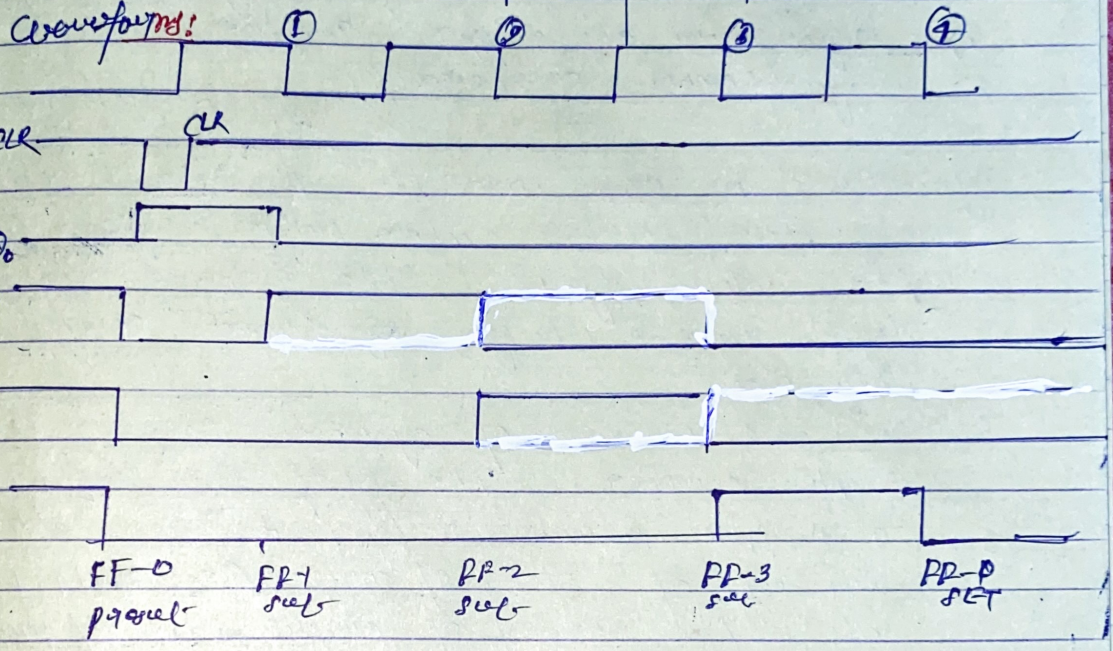


Fig: waveforms of ring counter.

Applications: There are following applications of shift registers.

i) For temporary data storage
ii) For multiplication and division
iii) As a delay line
iv) As a serial to parallel converter.
v) As a parallel to serial converter
vi) As ring counter
vii) As a twisted ring counter or Johon Counter
viii)